Notice of Allowability	Application No. 10/689,868	Applicant(s) SHIBATA ET AL.	
	Examiner Vu A. Le	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☒ The drawings filed on *20 October 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/358,643* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/20/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Vu A. Le
Primary Examiner

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: the present invention relates to a multi-bit memory device. The independent claims 1, 5, 8, 11 and 21 recites a multivalue memory device comprising first, second and third data storage circuit and a control circuit for writing data into first and second pages by storing the data in a second page into the second data storage circuit, storing the data in the first page into the first data storage circuit and setting the second logic level in the third data storage circuit in a case where data "2" has been written into the memory cell or a case data "1" has been written into the memory cell and a first verify voltage has been exceeded, and, in other cases, setting the first logic level in the third data storage circuit (claims 1 and 5) or storing the data in the first page into the second data storage circuit, transfers the data in the first page stored in the second data storage circuit to the first data storage circuit, storing the data in a second page supplied from the data line into the second data storage circuit, setting write data on the basis of the data in the first page stored in the first data storage circuit and the data in the second page stored in the second data storage circuit, and writes the data in the first page and the data in the second page into the memory cell at the same time on the basis of the write data (claims 1 and 8) or a write circuit for controlling the threshold voltages of said plurality of memory cells to write data and which includes a first step of, according to data to be written, keeping the threshold voltage of a first memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage to the third threshold voltage, a second step of, according to data to be written, keeping the threshold voltage

of a second memory cell at the first threshold voltage or changing the threshold voltage from the first threshold voltage the third threshold voltage, and a third step of, when the threshold voltage of the first memory cell is the first threshold voltage, according data be written, keeping the threshold voltage of the first memory cell at the first threshold voltage changing the threshold voltage from the first threshold voltage the second threshold voltage, and of, when the threshold voltage first memory the third threshold voltage, according to data to be written, keeping the threshold voltage of the first memory cell at the third threshold voltage or changing the threshold voltage from the third threshold voltage to the fourth threshold voltage, and which, when the threshold voltage of the first memory kept at the third threshold voltage in the third step, changes the threshold voltage of the first memory cell if the threshold voltage of the first memory cell has not reached a specific threshold voltage (claims 11 and 21). The PRIOR ART fails to disclose or suggest such a multivalue memory device as described in the independent claims 1, 5, 8 11 and 21, therefore, claims 1-30 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

03/18/05